ATLAS LAr FEB Testing and Qualification Procedures

J. Ban[1], D. Breton[2], F. Lanni[3], J. Parsons[1],
S. Rescia[3], S. Simion[1], D. Zerwas[2]

[1]Nevis Labs, Columbia University,
[2]LAL, Orsay,
[3]Brookhaven National Lab

March 8, 2004

Version 1.4

Abstract

A description is presented of the procedures and set of tests to be used in the QA/QC procedure for production of the Front End Boards for the ATLAS liquid argon calorimeter readout.

Contents

1 Introduction

The Front End Boards (FEBs) [1] of the ATLAS LAr calorimeter readout contain preamplifiers/preshapers, shapers, SCA analog memories, ADCs, and associated control logic. Each FEB comprises 128 readout channels.

The FEB production plan requires a total of 1627 FEBs to be produced. This total includes the set of 1524 FEBs required to instrument the various LAr calorimeters, a set of 87 spare FEBs, and an allocation of 16 FEBs (≈1%) which are assumed to be unrecoverable due to "infant mortality". The spare FEBs are to be fully tested and kept at CERN ready as spares for installation in ATLAS during maintenance periods. Therefore, a total of 1611 FEBs is to be tested and delivered to CERN. Table 1 documents the allocation of the FEBs, both installed and spare, to the various LAr calorimeters including electromagnetic barrel and endcap (EMB and EMEC), the hadronic endcaps (HEC), and the forward calorimeters (FCAL).

Calorimeter	Installed FEBs	Spare FEBs	Total
EM Barrel and Endcap	1448	74	1522
Hadronic Endcap	48	6	54
Forward	28	7	35
Totals	1524	87	1611

Table 1: Summary of the numbers of FEBs required to instrument the various LAr calorimeters, as well as the allocation of spare FEBs.

While all FEBs are produced from an identical set of printed circuit boards (PCBs), each FEB gets "customized" according to which section of the calorimeter it is reading out. This customization is performed in three distinct ways:

1. the analog input stage of the FEB incorporates preamplifiers (for the EM and FCAL) or preshapers (for the HEC), each of which exist in several distinct varieties,

2. the gain of the trigger sum from the linear mixer in each shaper can be set to one of two possible values,

3. the Layer Sum Boards (LSB) for forming analog trigger sums come in several distinct configurations.

It is important to note that the preamps/preshapers and LSBs are implemented as plug-in daughterboards and can therefore be manually installed, and changed if necessary, at any time after the FEB assembly. However, the linear mixer gain setting requires soldering of the appropriate jumper near each of the 32 shaper chips on a given FEB. Selecting the linear mixer gain setting will, therefore, be done as an "Assembly Option" at the time of the assembly (in industry) of the FEB PCBs.

2 FEB Production

The FEB is a large 10-layer PCB, with ≈ 200 active components and a total of over 20k solder joints. The complexity of the FEB, coupled with its stringent reliability specifications, requires tight quality control in all steps of the production process, including component delivery, PCB fabrication, and PCB assembly.

2.1 FEB Component Delivery

Each FEB includes ≈ 200 active components. These include a large number of custom components of different technologies, designed and developed by many different institutions. Individuals responsible for the delivery of each component have been identified.

To ensure high quality and high reliability FEB production, it is essential that certain requirements are met in the delivery of the components. These requirements include:

1. all custom components must be pre-tested by the responsible institution and only fully functional components accepted and delivered for FEB production

2. handling of components during pre-testing must be performed with great care to avoid damage to the component leads

3. in many cases, custom components will be labelled with individual serial numbers as part of the pre-testing process. In these cases, the labelling must be done in a way which will not interfere with industrial automatic pick-and-place and PCB assembly machinery. The institution providing the components is responsible for maintaining a database with the serial numbers and whatever other test data is relevant for a particular component.

4. components should be delivered in anti-static packaging

5. components should, if possible, be delivered in sealed moisture-resistant packaging, with the seal date noted

6. components must be delivered in trays or reels suitable for industrial automatic pick-and-place machinery. Care should be taken that the orientation of the components within the trays is consistent.

7. the component trays must be suitable for baking at 125 degrees Celsius in order to remove moisture from the components before PCB assembly

8. sufficient components are to be delivered to assemble the complete set of 1627 FEBs, plus an additional 8% allocation of spare components

9. to ensure no stoppage in the production flow occurs due to missing components, the full quantity of all active components except for the plug-in components (preamps, preshapers, LSBs) should be delivered to Nevis before the full FEB production is launched.

Nevis will store all the active FEB components. Upon receipt of the components at Nevis, a random sample will be inspected. After inspection, they will be once again vacuum-sealed in bags which include dessicant before being stored. The delivery from Nevis to the industrial assembler of all the active components required for assembly of a production FEB lot will be scheduled to keep the part delivery approximately one lot ahead of the assembly process. The assembler will be required to bake all component trays before proceeding with assembly.

Subject to negotiation with the assembly vendor, the assembler could directly procure and receive the passive components (resistors and capacitors). In this case, the full specification of all passive components, including vendor, type, value, and tolerance, will be coordinated with Nevis.

2.2 FEB Pre-Series Production

Before launching full FEB production, a pre-series production will be performed. Purposes of the pre-series include mastering the "learning curve" which is inevitable in the fabrication, assembly, and qualification of a board of this complexity. The pre-series FEBs will be subject to the same steps outlined below for the full production.

The pre-series FEBs will be included in the total of 1627 FEBs to be produced since, apart from being produced first, they will be identical to the FEBs from the full series production. The pre-series step will be included in the contracts negotiated with the industrial vendors selected for the FEB PCB fabrication and assembly.

A total of ≈ 20 FEB PCBs will be fabricated in the first step of the pre-series production. The pre-series assembly will proceed in two steps: initially, a single FEB will be assembled and delivered to Nevis. Assembly of the remaining FEBs will proceed only upon approval from Nevis, after successful testing of the first FEB.

It is likely that a single pre-series production will not be sufficient to fully qualify the FEB series production and assembly process. The production plan foresees several runs of $\approx$ 20-50 FEBs over a 2-3 month period, before the final production rate will be achieved. The purpose of these runs will be to ensure that the FEB production and assembly process is under control in order to achieve the required level of quality.

2.3 PCB Fabrication

The FEB PCBs will be fabricated in industry and delivered to Nevis in lots. The exact lot size and production schedule will be negotiated with the vendor. However, lot sizes of order 400 PCBs delivered once per month are reasonable estimates. The PCB fabrication schedule will be designed to stay reasonably ahead of the FEB assembly schedule.

The FEB PCB production order will require that the vendor perform full electrical testing of all bare PCBs. The "bed of nails" test will verify the continuity and isolation of all nets.

The FEB manufacturer will label each FEB PCB with a unique serial number. Each FEB will be individually wrapped in a protective plastic wrap before delivery to Nevis.

Upon receipt at Nevis, the serial numbers of the PCBs in each production lot will be recorded along with the lot number and date received.

To minimize handling of the bare PCBs, a subset of only a few PCBs per lot will be visually inspected to check the quality of the PCB fabrication. The inspection will check for flatness as well as overall quality and cleanliness. A few vias will be inspected under a microscope to check the alignment of the various layers. A limited number of Ohmmeter tests will also be performed to check for shorts and for continuity.

Accepted PCBs will be delivered from Nevis to the assembler in lots, matching the delivery of the active components. The serial numbers of the PCBs of each assembly lot will be recorded before delivery to the assembler.

2.4 PCB Assembly

FEBs will be assembled in industry in lots. The exact lot size and delivery schedule is subject to negotiation with the vendor. Preliminary discussions with potential vendors suggest that, once the full production rate has been achieved, it is likely that lots of ≈ 100 FEBs will be assembled each week. This rate would allow completion of the FEB assembly order on a timescale significantly less than one year.

The industrial assembler will be responsible for the complete assembly of the FEB, apart from plugging in the preamplifiers/preshapers and LSBs. The assembly will include mounting all connectors, connector shields, and preamp Faraday shields. The front panel with its cooling block attached will also be mounted, along with all the stand-offs for the cooling plates. FEBs will be delivered to Nevis ready for testing, with no additional assembly required.

The assembly contract will require the PCB assembler to perform a fully automated visual inspection of each FEB after assembly. The inspection will verify the presence and correct orientation of all components, as well as visually inspect all solder joints. In addition, a fully automated X-ray inspection of all solder joints is being negotiated, searching for opens and shorts and also verifying the presence of sufficient solder as well as the solder profile.

A critical feature of the QA/QC process for the FEB production is that each delivered lot is validated before the next lot is assembled. A quality control goal will be negotiated with the vendor, along with a cut-off date by which they have to be informed of a quality problem in order to interrupt the production process before assembly of the next lot. The validation will be performed by randomly selecting $\approx$ 5-10% of the FEBs of each lot, and subjecting them to the full testing procedure described in section 3. Due to the time-critical nature of the validation process, this sample testing will be performed at Nevis.

3 FEB Testing and QA/QC Processes

The process of testing and qualifying the full set of 1627 FEBs will follow a well-defined sequence of steps and tests. The proposals presented represent a reasonable baseline for the tests to be performed, based on our current knowledge. Results from the pre-series experience will be used to fine-tune the production cycle (for example, the duration and exact specifications of the burn-in process).

3.1 Organization of the Work

The task of testing the full set of FEBs will be shared between Nevis, LAL and BNL. Nevis will provide overall coordination of the FEB production and testing, and perform all interactions with the industrial vendors.

The sequence of steps, each of which is described in more detail later, is as follows:

Steps performed at the PCB assembler

1. Automated Inspection

   The PCB assembly process will include aotumated visual inspection of all FEB components and solder-joints. The possibility to perform a full automated X-ray inspection is also being discussed with possible vendors.

2. Initial Power-On Sequence

   GPIB-controller power supplies are used to power an FEB for the first time. Controlling the current limits seeks to reduce or eliminate damage in case of a short or other problem. Any FEBs which fail this step will be set aside and sent to Nevis for debugging.

3. Digital Test

   The digital functionality of the FEB is tested and verified. Limited information about the performance of the analog chain beginning with the shaper is also obtained and evaluated. Any FEBs which fail this step will be set aside and sent to Nevis for debugging.

4. HASS testing and Burn-in

   FEBs are subject to a highly accelerated stress screening (HASS) and burn-in process in order to identify failures and infant mortality.

5. Post-Burn-In Digital Re-Test

   The digital test is repeated to search for failures which occurred during the burn-in. Any FEBs which fail this step will be set aside and sent to Nevis for debugging.

Steps performed at Nevis

1. Inspection and Acceptance

   As each FEB is received at Nevis, it will be subject to an acceptance test. This step will include inspection of the FEB, and verification of its required data in the production database.

   The serial numbers of the digital components to be recorded will be entered into the production database.

2. Timing Measurements

   The frequency range over which the on-board QPLL properly locks will be measured. In addition, the jitter spectrum of the FEB output optical data will be measured.

3. Sample Measurements

   A sample of $\approx 10\%$ of FEBs will be configured with preamps and LSBs and subjected to the full set of tests described below in order to ensure the required quality of the assembly and test process is being maintained.

Steps performed at BNL/LAL

1. FEB Configuration

   Each FEB is configured specifically for its intended location in the detector by installing the appropriate plug-ins (preamplifiers/preshapers and LSBs).

2. Analog Test

   A set of calibration tests is performed to verify the required analog performance through the entire analog chain of the FEB.

3. Cooling Plate Installation and Qualification

   The cooling plates are installed, after which a vacuum test is performed to verify the tightness of the connections and cooling system.

4. Final Test

   The final FEB acceptance test is performed, before shipping the FEB to CERN for installation.

For each step, a set of criteria will be specified to clearly define what is required to consider that an FEB has passed a particular test, and the remedial actions in case of a failure.

In addition to defining a rigorous QA/QC procedure, an important goal is to identify FEB problems early in the testing process, both to minimize possible damage to boards and components, and to provide a time- and manpower-efficient FEB production cycle.

3.2 Inspection

The FEB assembly process will include automated visual inspection of all FEB components and solder joints. The possibility to also perform automated X-ray inspection is being discussed, though the large size of the FEB might prevent a full X-ray inspection.

3.3 Initial Power-On Procedure

To limit the possibility of damage to components occuring due to undetected shorts or other problems existing on a previously untested FEB, the power will be turned on in a controlled way when powering a new FEB for the first time. The programmable current limits on the power supplies will be used to prevent excessive currents, and the power-on sequence will be terminated should the DAQ PC detect that any of the currents are rising beyond a reasonable range.

Once the power supplies have reached their nominal voltages, the currents will be recorded in the FEB PDB. Any FEBs for which the power-on sequence is prematurely terminated will have the voltages and currents recorded with the error condition, and will be set aside to be sent to Nevis for debugging.

3.4 Digital Test

The next step in FEB testing will be to verify the proper logical functionality. This digital testing proceeds in several phases. First, the distribution of clock and control signals is checked by verifying that the TTCRx has detected the clock, and then using the SPAC link to check the communication will all the configurable devices on the FEB:

- verify that the two front panel LEDs connected to power are asserted
- check that the TTCRx is locked on the incoming TTC signal by verifying that the front panel LED connected to the TTCRx Ready signal is asserted
- verify that the FEB responds to SPAC commands to its address as well as to Broadcasts
- enable, via SPAC, all on-board regulators which are configured to be inhibited upon power-up
- record the supply currents once all regulators are enabled, and verify they lie within the acceptance windows defined
- verify that the SPAC can communicate with each of the two DCU chips, and use the DCU chips to measure the on-board temperatures and monitored voltages
- verify the capability to download and readback via SPAC the switch settings for the linear mixers in the 32 shaper chips
- verify the capability to download and readback via SPAC the configuration parameters for each of the 8 Gain Selectors
- verify the capability to download and readback via SPAC the configuration parameters for each of the 2 SCA Controllers

The next set of digital tests is to check that the optical link between the FEB and ROD is functional:

- check that the optical link on the FEB is properly locked by verifying that the FEB front panel LED connected to the GLink Lock signal is asserted
- check that the optical link on the ROD is properly locked by verifying that the ROD front panel LED connected to the GLink Lock signal is asserted
- verify that the correct data is received at the ROD when the FEB is triggered after being configured in "test data" mode

In the final phase, the FEB is triggered in various configurations and the output data examined for possible anomalies. The FEB should be configured to data taking mode instead of test data. The FEB configurations which should be verified, with both 5 and 32 sample readout, include:

- single fixed gain, HI gain only
- single fixed gain, MED gain only
- single fixed gain, LO gain only
- three fixed gains, HI/MED/LO gains
- single auto-gain with thresholds set such that HI should be selected
- single auto-gain with thresholds set such that MED should be selected
- single auto-gain with thresholds set such that LO should be selected

The FEB data verification performed at the ROD should check that all header and trailer words are correct. In addition, while the FEB at this stage of testing is still missing the preamps/preshapers, calculation of the means and RMS's of the pedestal distributions is sensitive to many possible problems in the proper analog functioning of the combination of shaper + SCA + opamps + ADC. For example, it should be possible to detect the influence of the shapers on the noise in the HI and MED gain settings.

The test will be fully automated, and operated by a technician at the assembler in Pass/Fail mode. Results from the test will be automatically written to the database.

Boards which fail the test will be sent to Nevis for debugging; once repaired, they will be returned to the assembler and moved to the HASS/burn-in step described below.

3.5 HASS Test and Burn-In

The goals of a burn-in include the detection of weak or faulty solder joints, as well as instances of component infant mortality. Highly Accelerated Stress Screening (HASS) techniques have been developed in industry to effectively detect such problems. Random vibration tests reveal solder joint problems, as well as bonding or mechanical defects in components. Thermal cycling stresses components in order to reveal infant mortality problems.

Given the automated inspections of each FEB which will be performed by the PCB assembler, the rate of solder problems is expected to be rather low. However, since the

majority of FEB active components are custom devices, it is difficult to estimate the rate of component infant mortality failures to expect.

The large number of custom devices also makes it difficult to reliably predict the exact type and duration of burn-in which will be required to effectively eliminate infant mortalities. To gain some experience, we have performed extensive HASS-style tests on two pre-series FEBs which could be spared; a description of the tests performed can be found in reference [2]. Those tests support the notion that the baseline HASS proposal described below would not significantly degrade the lifetime of the production FEBs. However, given the low statistical power of the sample of FEBs tests, plus the fact that the two FEBs in question had already been operated extensively in the lab, we cannot yet know whether the baseline proposal is sufficiently rigorous to efficiently reveal infant mortality problems. The efficacy of the HASS process will have to be evaluated, and the procedures refined, as production is underway.

For planning purposes, we adopt a baseline proposal, based on previous experience as well as a reading of the literature, to subject each FEB to a combination of vibration tests followed by thermal cycling:

1. Vibration test
    - random vibrations about 3 axes
    - frequency limits: 10 - 1000 Hz
    - spectral density = 10g RMS
    - duration = 10 minutes
2. Thermal cycling
    - temperature cycle of 100 minutes at 55 deg C, followed by 20 minutes at 0 deg C
    - rate of temperature change = 10 deg C/minute
    - number of cycles = 4
    - during the thermal cycling test, the FEBs will be powered, clocked, configured, and provided with triggers, in order to fully exercise all the components
    - total duration = 8 hours

Details about the HASS procedure and duration applied to each FEB will be entered into the FEB PDB, along with the date the procedure was performed.

In addition to the HASS procedure applied to all FEBs, it is planned to subject a subsample of the first few production lots to a more "traditional" burn-in test, such as operation at 55 deg C for a period of 168 hours. This investigation will be used to further validate the effectiveness of the HASS test at eliminating problems which would be discovered during the burn-in.

3.6 Post-Burn-in Digital Re-Test

After the burn-in procedures, FEBs will be subjected again to the digital test described previously in order to detect any failures which were induced by the burn-in. Any failures will be entered in the FEB PDB in order to be able to search for and track possible trends in failure modes.

Boards which fail the test will be sent to Nevis for debugging and repair, after which they will be re-tested at Nevis. Once an FEB passes the test, it will be moved to the next step.

3.7 Acceptance

Upon receipt at Nevis, assembled FEBs will be subject to an acceptance process. First, the FEB serial number will be checked against the FEB PDB to ensure that an assembly lot includes all of the FEBs expected. The database will be updated with the date the assembled FEB was received. A check will be made that the required data from the testing at the assembler has been entered into the database.

A visual inspection will then be performed. While it is impractical to inspect any sizeable fraction of the $\approx$ 20k solder joints on each FEB, the visual inspection will include the following requirements:

- inspect the overall board for quality (eg. flatness, cleanliness, lack of visible damage)
- verify the correct jumpers have been soldered for setting the gains of the linear mixers
- verify that all diodes and any polarized capacitors have been soldered in the correct orientation
- examine under a microscope a limited number of soldered pins

As part of the inspection, the serial numbers of certain digital components will be entered into the FEB PDB. The list of digital components for which this information should be recorded is still to be decided, and will be discussed with the institutions providing the various components. It is expected, for example, to record the serial number of the SMUX and the OTx, for which detailed measurements will be available. Most of the other digital components are produced in a single lot, and it is likely not necessary to record the serial numbers of chips on a particular FEB.

The date/time of the acceptance test, as well as the name of the operator, will be entered in the FEB PDB.

3.8 Timing Measurements

The absolute frequency range over which the on-board QPLL locks will be measured for each FEB, with the results recorded in the database. Cuts will be made on both the width of the operating window, and also the absolute frequencies in order to ensure sufficient operating margin with the LHC frequency.

A measurement of the jitter spectrum of the output optical data will also be made and recorded. It is expected that the presence of the QPLL will provide quite uniform performance for all FEBs. Should this prove to be true, this time- and manpower-intensive step could be eliminated at some point, and only performed on a sample of FEBs as a cross-check.

3.9 FEB Configuration

Once an FEB has successfully passed all the previous tests, it must be equipped with the appropriate combination of preamps/preshapers and LSBs. (Note that these plug-in components have been separately burned in during their production testing, and therefore do not need to be installed before the FEB burn-in.) The FEB PDB will be updated at this time with the types and serial numbers of these components, as well as of other relevant analog components (shapers, SCAs).

3.10 Analog Test

To test and evaluate the analog performance of the FEB, detector simulation boards will be connected to the FEB input connectors, allowing noise measurements and signal injection in an ATLAS-like way. Reference values and acceptance windows for all foreseen measurements will be defined as a function of the preamp/preshaper flavor based on results obtained with the pre-series FEBs.

After the FEB is powered on, all voltage regulators will be enabled. The power supply currents will be measured and recorded in the FEB PDB. Based on the experience gained with the Module 0 FEBs, several different types of runs will be performed to test the analog performance of the FEB.

- Pedestal runs

  The pedestals, noise and fixed sequences noise (FSN) will be measured and compared to the nominal values. The measurements will be performed separately for the High, Medium and Low gains. Dead channels will be easily detected via (too) low noise. The noise is also sensitive to the time constant of the shaper. The FSN measures the pedestal dispersion of the 144 capacitors of the SCA.

  An analysis of coherent noise will be performed, including summing over all 128 channels, as well as analyzing smaller subgroups of channels (64, 8, and 4). The input connectors to the FEB are shielded in order to provide some sensitivity to coherent noise. However, since the FEB is not installed during testing in a front end crate with final baseplane, the complete grounding configuration is not fully tested.

- Calibration pulse runs

  Calibration pulses injected to the FEB will be used to test and evaluate the analog functionality and performance. For each test, means and RMSs will be calculated for the samples, as well as for the optimally filtered pulse. The means provide checks of signal shapes, amplitudes and timing, while the RMSs provide sensitivity to other parameters affecting the energy and time resolution, such as timing jitter.

A number of different pulse tests are performed in order to evaluate the required list of functionality and performance parameters:

- Timing runs

  All channels are pulsed simultaneously. The three gain scales are calibrated separately, with a DAC value chosen appropriately for each gain scale to give an almost full height signal. The full signal waveform will be recorded as the calibration pulse delay is incremented with a step size of less than 1 ns. The signal form will be compared to the reference signal. The position of the maximum amplitude in time will be analysed to detect incorrect peaking times (a problem which occurred for some Module 0 shapers). The signal form analysis also verifies the read and write operations of the combination of SCA Controllers, SCA address bus and SCA chips.

- Ramp runs

  Calibration pulses will be measured for a variety of DAC values. The gains of each channel and gain will be calculated and compared to the nominal values, allowing the detection of dead channels and channels with linearity problems.

- Crosstalk runs

  One out of 8 FEB channels will be pulsed at once, with a fixed DAC value chosen appropriately for each gain scale. Measurements of the magnitude and shape of crosstalk will be made, typically using 16 time samples.

- Autogain runs

  A ramp run is performed with the Gain Selectors of the FEB configured for autogain selection, in order to verify the proper operation of the gain selection algorithm.

In addition to evaluating the analog performance of the readout channels, the trigger sum outputs are also checked. The gains of the trigger sum outputs will be measured. The correct functioning of the shaper switches will be tested by checking the amplitude of the trigger outputs as a function of the number of channels with the switch set to "ON" via SPAC for a given trigger output. The shape of the trigger sum output signals must also be verified.

3.11 Cooling Plate Installation and Qualification

The assembly of the cooling circuit on the boards foresees the following procedures (for each side of the board):

1. Cooling block installation: the cooling block will be attached to the front panel by 3 screws. The O-rings will be inserted in the cooling block grooves

2. Preparation and assembly of the thermally conductive plastic: A thin layer of thermally conductive material (Berquist Gap Pad V0 Soft) will guarantee a proper thermal path to the cooling circuit. The material comes in 8"x16" sheets (0.02" thick) pre-cut in strips or in pads to be attached on all the high power active components on the boards.

3. Assembly of the heat transfer plates: The alignment of the plate is easily realized through the oversized holes corresponding to the standoffs.

4. Installation of the cooling plate: The plate is aligned to the board standoffs and to the corresponding holes in the cooling block. 52 brass screws will guarantee uniform pressure on the whole FEB area.

5. Installation of the pipe and fittings to the manifolds: Taigon pipes will have to be cut in the proper length and mounted on the cooling block nipples. Quick insertion fittings have to be mounted on the other end.

After the installation of the two sides has been completed, the assembly will have to be leak tested. Tests have been run at BNL where the cooling assembly was either pressurized to a max of 3 bars (50psi) or connected to a poor vacuum pump. A pressure gauge can easily detect leaks (in about 5 to 10 minutes) after the pressurizing system or the vacuum pump has been disconnected.

3.12 Final Test

Before shipment of the FEBs to CERN for installation, a final test will be performed to verify that no damage was caused during installation of the cooling plates. The final test will include selected aspects of both the digital and analog tests described previously.

It is possible for a test setup where multiple FEBs can be tested simultaneously, such as at BNL, that the cooling plates could be installed before performance of the analog tests, and the analog testing be combined with the Final Test after cooling plate insertion. This approach could reduce the testing time required if experience with the first FEBs demonstrates that a sufficiently small fraction FEBs demonstrate problems which are detected only during the analog test (for which the cooling plates would have to be removed and later installed).

4 FEB Long-Term Burn-In Tests

With FEB production slated to begin in mid-2004, it is possible to continuously operate a set of FEBs for a period of almost 3 years before the LHC turn-on. Experience gained in this way would prove very valuable in evaluating the long-term reliability and maintenance requirements of the FEBs.

The FEC system crate test setup at BNL could be used to perform such long-term burn-in tests of the FEBs, as well as other boards in the LAr front end crate. Utilizing one of the crates for production FEB testing would still leave one crate, which holds 28 FEBs, available for long-term tests.

An additional use of such a testing setup would be the ability to do "system tests" on production FEBs, similar to what is planned for the FEC system test. The crate could be loaded with appropriately configured FEBs in order to mimic the readout of a particular section, or sections, of the calorimeter. Crate-level tests, such as measurement of coherent noise, could check that the production FEBs continue to meet the specifications and reproduce the results of the FEC system test.

5 FEB Production Schedule

As discussed previously, several "pre-series" runs of 20 - 50 FEBs will be used over 2 - 3 months to set up and qualify the FEB production process. Once the process is qualified, a steady-state production rate of 100 FEBs per week will be followed. This rate is estimated by possible assembly vendors to be ideal for maintaining very high quality in the assembly process. With this plan, the total production of 1757 FEBs will take approximately 7 months.

The baseline HASS proposal would allow one set of 16 FEBs to be burned in each working day. Allowing for some inefficiency, we estimate 64 FEBs can be cycled through the HASS system each week. While this is sufficient to keep up with FEB pre-series production, it is not possible to keep up completely with the steady-state FEB production rate in real time. Instead, a little more than half of the FEBs produced each week would be subject to the HASS test the following week, in order to qualify the lot. The additional FEBs would be put aside and tested later, when FEB production has been completed.

It is estimated that the procedures to be completed at Nevis on all FEBs can be performed on 10 FEBs per day, for 50 FEBs per week. To allow for some inefficiency, we assume 40 FEBs per week. It should be noted that debugging and repair of faulty FEBs will be performed in a different test setup at Nevis, and with different people, in order not to interfere with the steady rate of FEB acceptance tests. The test setups at BNL and LAL can handle the assumed delivery rate of 20 FEBs per week at each site.

Putting together the various steps in the FEB production and qualification process, the schedule requires a total of period of approximately 14 months is required from the beginning of the pre-series production until the completion of the FEB testing and qualification.

6 FEB Installation

To streamline the FEB installation work at CERN, it is planned to ship to CERN groups of FEBs arranged according to their eventual location on the detector. The typical FEB shipment to CERN would include all FEBs required to fully equip one half-crate of the detector, organized according to the slot into which each individual FEB should be inserted.

FEBs will be received at the LAr Electronics Maintenance Facility (EMF) being set up at CERN, where the final preparations will be made for installation. The steps to be taken are the following:

- unpack each FEB from its individual shipping box
- update the FEB PDB to indicate the board has been received at CERN, and the date of reception
- verify with a water test that the cooling plates and connections are still water-tight
- insert the FEB in the appropriate slot of the FEC installation carrier
- complete the TC "passport" for each board, required as part of the Installation Database
- transport the carrier from the EMF to the ATLAS pit, and install all boards in the appropriate crate and slot.

It should be noted that it is not expected to require that the FEBs be re-tested at CERN before installation on the detector, with the exception of the water test. The implications of experiencing a water leak in a front end crate on the detector are sufficiently hazardous that it is prudent to verify the leak-tighness of the cooling before moving boards to the pit. However, it is believed that the FEB itself is sufficiently robust, particularly having passed through the burn-in and testing procedures, and the possibility of damage during shipment sufficiently low, that it is not necessary to power on and test the FEB at CERN before installation. Since the LAr EMF will be fully functional well before FEB installation begins, it will be possible to verify this conclusion by re-testing at CERN a sample of FEBs delivered early in the production cycle. The possible tests which would be performed are described in the note on the front end electronics installation planning[3].

References

[1] J. Ban, S. Negroni, J. Parsons, S. Simion, and B. Sippach, "Design and Implementation of the ATLAS LAr Front End Board"; available at `http://www.nevis.columbia.edu/~atlas/electronics/ATLASFEB/FEBnote.pdf`.

[2] G. Brooijmans, D. Dannheim, I. Katsanos, and J. Parsons, "Accelerated Stress Tests of ATLAS LAr FEB Prototypes"; available at `http://www.nevis.columbia.edu/~atlas/electronics/ATLASFEB/hassnote.pdf`.

[3] Note on FE installation.